REMARKS

Below, the applicant's comments are preceded by related remarks of the examiner set forth in small bold type.

> **Claims 1-6 and 8-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Glew et al. (5,561,780) in view of "The Cache Memory Book" by Jim Handy.**
>
> **Regarding Claims 1-6 and 10, Glew et al. teaches a buffer 132 ("cache") with a number of cache-line sized storage locations 136 ("cache lines") and an eviction unit 139 enabled to evict data from the storage locations when partial writes fill a single storage location one storage portion 140 ("cache line has multiple portions") at a time. A thirty-two-byte validity filed 144 ("validity bit storage") keeps track of which of the thirty-two portions of each storage location has been written to and when all are full, the storage location ("cache line") is evicted (See Figure 4 and Column 4, lines 59-67 and Column 7, lines 1-30). Glew et al. also discloses that storage in the buffer 132 is very much like storage on an on-chip cache unit (DCU), therefore, as DCU's, buffer 132 may store data corresponding to locations in main memory (See Column 1, lines 25-38 and Column 7, lines 30-32). Glew et al. does not teach buffer 132 being part of a coherency protocol. Handy teaches cache coherency which prevents stale data from being confused with current data (page 124). It would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate the cache coherency of Handy to the buffer of Glew et al. since this buffer behaves much like a cache and adding such protocol would prevent the confusion between good and useless data. It is understood that in integrating a cache coherency protocol to the invention of Glew et al., small delays in between data evictions must be added; adding such delays would be a tradeoff to be paid for the ability to differentiate between stale and current data.**

The examiner acknowledges that Glew does not teach the buffer 132 (which stores uncacheable data) being part of a coherency protocol, but contends that combining Handy's cache coherency with Glew would have been obvious. Yet the examiner's position fails to give proper weight to what Grew himself says about cache coherency, which would have made a combination of Handy and Glew quite unobvious.

As Glew explains with respect to coherency, "processor ordering is ignored

for writes from the write-combining buffer. No delay between consecutive partial write operations is required since global observability is no longer necessary. ... no read-for-ownership or similar operation need be performed to read an entire line of uncacheable data into the write combining buffer." (col. 10:16-22) This is desirable because "a substantial reduction in graphics bandwidth is achieved." (col. 5:26-27)

In fact, Glew teaches away from operating the buffer in compliance with a cache coherent protocol: "[F]or data wherein the programmer wishes processor ordering to be preserved, the associated value is set to ensure that the data is not stored within the write-combining buffer and hence is not subject to a possible violation of processor ordering." (col. 11:58 to col. 12:2) In other words, if the programmer wants cache coherency to apply, he is told by Glew to make sure that the data is not stored in the buffer.

The examiner accepts that making the Glew buffer comply with a cache coherent protocol would add delays but asserts that "adding such delays would be a tradeoff to be paid for the ability to differentiate between stale and current data." However, because all of the data stored in the write-combining buffer are going to be used in a later step, there is no reason to differentiate between stale and current data. The data are all current and are all sent to the display device 124. Therefore, adding the delays as suggested by the examiner would not represent a "tradeoff" because there simply is no countervailing benefit to be achieved in exchange for the cost of the delays.

Claims 2-6 and 10 are patentable for at least the same reasons as claim 1.

> **Regarding Claims 13, 15, 18, 22-26 and 28, Glew et al. teaches a buffer 132 ("cache") with a number of cache-line sized storage locations 136 ("cache lines") being written to through the use of a write combining unit 138, and an eviction unit 139 enabled to evict data from the storage locations when partial writes fill a single storage location one storage portion 140 ("cache line has multiple portions") at a time. A thirty-two-byte validity filed 144 ("validity bit storage") keeps track of which of the thirty-two portions of each storage location has been written to and when all are full, the storage location ("cache line") is evicted (See Figure 4 and Column 4, lines 59-67 and Column 7, lines 1-30). Glew et al. also discloses that storage in the buffer 132 is very much like**

storage on an on-chip cache unit (DCU), therefore, as DCU's, buffer 132 may store data corresponding to locations in main memory (See Column 1, lines 25-38 and Column 7, lines 30-32). Glew et al. does not teach buffer 132 being part of a coherency protocol. Handy teaches cache coherency which prevents stale data from being confused with current data (page 124). It would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate the cache coherency of Handy to the buffer of Glew et al. since this buffer behaves much like a cache and adding such protocol would prevent the confusion between good and useless data. It is understood that in integrating a cache coherency protocol to the invention of Glew et al., small delays in between data evictions must be added; adding such delays would be a tradeoff to be paid for the ability to differentiate between stale and current data. Additionally, although the write transaction of Glew et al. are not initiated directly by a input/output device, these transactions, which are initiated by a microprocessor, could be initiated indirectly, through the microprocessor, by the input/output device 125 (Figure 3).

Claims 13, 15, and 18 are patentable for at least the same reasons as claim 1.

Claim 22 recites "initiating write transactions by an input/output device to write data." The examiner acknowledges that Glew does not disclose initiating write transactions by an input/output device, but contends that write transactions could be initiated indirectly, through the microprocessor, by the input/output device 125. The examiner's speculation, even if true, that Glew's write transactions could be initiated indirectly is insufficient to establish that doing so would have been obvious from Glew. In this regard, the applicant notes the portion of the applicant's background that states: "Data caching is typically not done when input/output (I/O) devices write data to main memory because it is unlikely that another transaction will involve the same address as the data previously written by I/O devices. Therefore, a computer chipset that manages data transfers to and from I/O devices typically forwards the write data directly to main memory without caching the data." (page 2, lines 4-7)

The applicant respectfully requests the examiner to support his assertion by indicating which passages in Glew would have made obvious the portions of the applicant's claim that recite: "initiating write transactions by an input/output device to write data [and] writing the data into a cache memory."

The remaining dependent claims are patentable for at least the same reasons

as the claims on which they depend.

The fact that the applicant has given replies to certain arguments of the examiner does not mean that the applicant concedes any other arguments of the examiner. The fact that the applicant has argued for the patentability of certain claims, does not mean that there are not other good reasons for the patentability of those claims, or other claims.

Please apply any charges or credits to deposit account 06-1050, referencing attorney docket 10559-639001.

Respectfully submitted,

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** See attached document certifying that Rex Huang has limited recognition to practice before the U.S. Patent and Trademark Office under 37 CFR § 10.9(b).*

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Expires: May 16, 2004

Harry I. Moatz
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